Peak-Efficiency Detection and Peak-Efficiency Tracking Algorithm for Switched-Mode DC–DC Power Converters

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***Abstract*—In this paper, the system allowing to detect the peak-efficiency point of the periodically switching MOS power transistor is presented. The use of this system concerns namely the integrated dc–dc converters, charge pumps, class-E amplifiers, or isolated MOSFET power switches. Information about the peak-efficiency point position can be used to modify the power-switch operating conditions, which allows us to obtain the maximal available power-efficiency for a given operating point. The algorithm of the peak-efficiency tracking is developed here on the example of integrated 3.2 MHz step-down (buck) 5-A dc–dc converter. In this example, sizes of NMOS and PMOS power transistors are adjusted "on the fly," in order to obtain the highest possible efficiency. In particular, power efficiency is optimized for the output current I_{OUT}, battery and output voltages V_{BAT} and V_{OUT}, switching frequency f_{SW}, temperature, and process variations. The principle of the method relies on the balancing of the Joule heat energy dissipated on the resistive elements, and energy dissipated during the charging process of the transistors' driving capacitances. As the result of the peak-efficiency tracking algorithm, the flat efficiency curve is obtained in a wide current range.**

***Index Terms*—High-efficiency dc–dc converter, peak-efficiency detection, power efficiency optimization.**

I. Introduction

ONE of the fundamental formulas in a dc–dc converter design stands for the power losses obtained as the sum of switching (dynamic) and ohmic (Joule) losses [1], [2]. This formula relies on the parasitic resistances including intrinsic NMOS and PMOS channels ON resistances $R_{\mathrm{ON}(N)}$ and $R_{\mathrm{ON}(P)}$, resistances of all metallic connections including R_{COIL}, on the driving capacitances $C_{G(N)}$ and $C_{G(P)}$ of power transistors, as well as on the output-node capacitance C_{LX}. From these parasitic elements, the power-efficiency curve can be obtained as the function of the output current I_{OUT}.

Typically, the efficiency curve has a low-current regime where the capacitive (dynamic) losses dominate, and a high-current regime where the ohmic-losses dominate. At very-low current regime (i.e., below the CCM/DCM boundary), the efficiency is usually improved by using low-frequency *pulse-skipping* (PSK) or *pulse-frequency modulation* (PFM) modes [14].

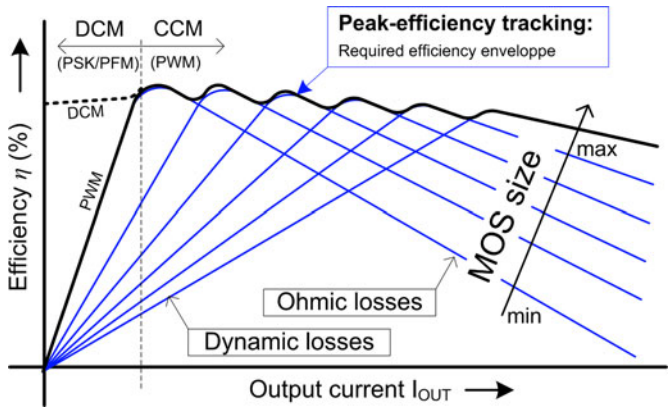

Fig. 1. Required performances of the peak-efficiency tracking algorithm. Size of the segmented power stage is adjusted in order to reach maximum available power efficiency for given output current I_{OUT}, V_{BAT}, V_{OUT}, temperature, f_{SW}, and process.

At an intermediate level, the power efficiency reaches maximum (peak) efficiency $\eta_{\max}$. The goal of the concept presented here is to accurately detect the position of this peak-efficiency point by an analog circuit. By using this information, operating conditions of the power switch can be adjusted. This adjustment allows us to trace the maximum efficiency together with the power-switch operating point. As shown in Fig. 1 (a), the "flat" efficiency curve for the low and intermediate current area can be obtained in PWM mode. The gain of the power-efficiency optimization can reach up to 10%, depending on the duty-cycle range D, and MOS power switch operating conditions (see measurements shown in Fig. 6).

An additional benefit of the peak-efficiency tracking algorithm is the improvement of the CCM/DCM boundary or zero-inductor current crossing detection accuracy. This is helpful mainly for the high-output current power stages [14], where the control of the low-power conduction modes (PSK, PFM) becomes difficult. Indeed, the peak-efficiency tracking algorithm increases progressively the $R_{\mathrm{ON}(N)}$ with decreasing output current I_{OUT}. This allows us to generate higher $V_{\mathrm{DS(ON)}}$ voltage across the NMOS power switch, which facilitates the accurate zero-current detection.

A. Lossy Power-Stage Model

In order to describe the concept of the peak-efficiency detection, a detailed view of the step-down (buck) dc–dc converter

Manuscript received October 10, 2013; revised December 10, 2013; accepted January 23, 2014. Recommended for publication by Associate Editor D. Maksimovic.

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Digital Object Identifier 10.1109/TPEL.2014.2304491

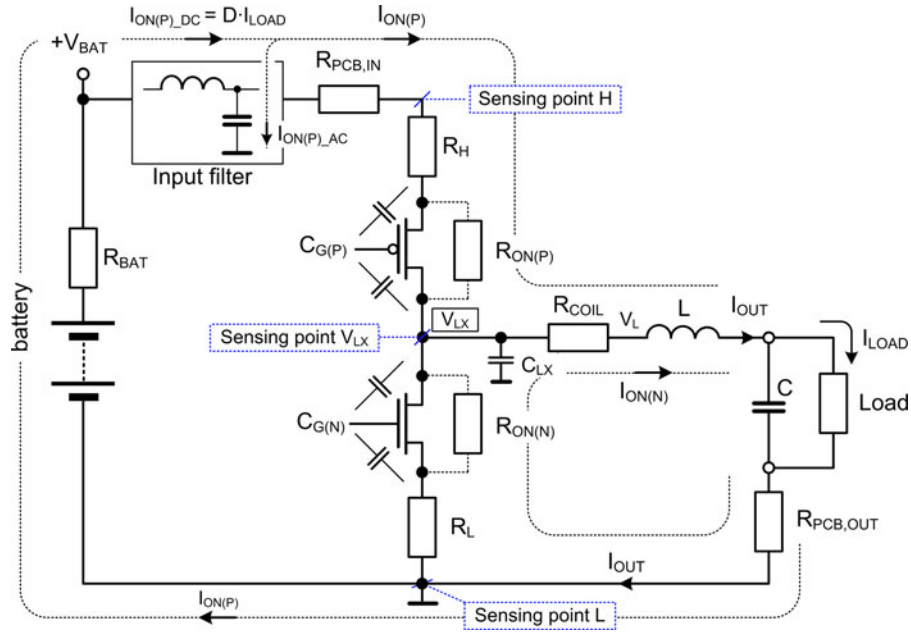

Fig. 2. Representation of the dominant ohmic and capacitive lossy elements in the buck converter power stage with highlighted paths of NMOS and PMOS switching currents.

power stage containing dominant parasitic lossy elements is shown in Fig. 2.

In this schematic, two current paths are highlighted: current path $I_{\mathrm{ON}(P)}$ of the PMOS transistor switch present during the PMOS conduction phase, and current path $I_{\mathrm{ON}(N)}$ of the NMOS transistor switch present during the NMOS conduction phase. $R_{\mathrm{ON}(N)}$ and $R_{\mathrm{ON}(P)}$ are the channel ON resistances of the power transistors, R_H and R_L are source and drain metallic access (layout) resistances, and R_{COIL} the dc resistance of an inductor. Resistances $R_{\mathrm{PCB,IN}}$ and $R_{\mathrm{PCB,OUT}}$ stand for the sum of all remaining input and output wiring resistances, which are encountered in the $I_{\mathrm{ON}(N)}$ and $I_{\mathrm{ON}(P)}$ current paths (e.g., PCB trace resistance, package access resistances, input filter, or even the battery output resistance). C_{LX} is the output node capacitance, which is usually dominated by the sum of NMOS and PMOS drain overlap and junction capacitances C_{DOV} and C_{Dj}.

Fig. 2 schematic can be simplified into schematic shown in Fig. 3. Here, R_N and R_P stand for the sum of all resistances related to the Joule losses of NMOS and PMOS conductive phases (i.e., $I_{\mathrm{ON}(N)}$ and $I_{\mathrm{ON}(P)}$ current paths). The values of R_{N_SWITCH} and R_{P_SWITCH} correspond to the resistances of switches inside the package (MOS R_{ON} with metallic access resistance), and value of $R_{(N,P)\_\mathrm{EXT}}$ to the sum of all external resistances. The sensing points refer to the nodes, where the voltage can be accurately measured and their use will be shown in the following.

The aforementioned formula for the power losses in the switched-mode power converter is usually written in the form [1]

$$P_{\mathrm{LOSSES}} = R \cdot I_{\mathrm{OUT}}^2 + C V_{\mathrm{BAT}}^2 f_{\mathrm{SW}}. \tag{1}$$

When focusing to the step-down dc–dc converter, value of R corresponds to the average "output" resistance of the power

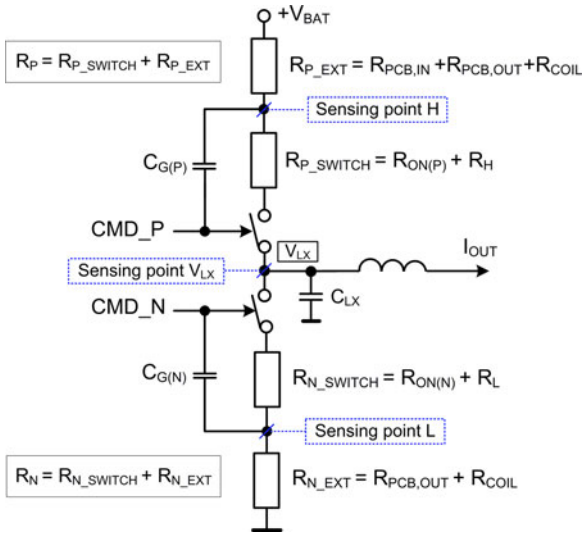

Fig. 3. Simplified representation of dominant ohmic and capacitive lossy elements in the buck converter power stage shown in Fig. 2.

stage $R = \mathrm{D}R_P + (1-D)\,R_N + R_{\mathrm{COIL}}$, and C stands for the sum of all parasitic capacitances being charged/discharged with switching frequency $f_{\mathrm{SW}} = f_{\mathrm{CLK}}$. The value of RMS output current I_{OUT} in (1) is affected by inductor triangular ripple current ΔI_L and can be expressed as

$$I_{\mathrm{OUT}} = \sqrt{I_{\mathrm{LOAD}}^2 + \Delta I_L^2/12}. \tag{2}$$

It can be shown that for $I_{\mathrm{LOAD}} > \Delta I_L/2$ (i.e., above CCM/DCM boundary, see Fig. 1), currents I_{OUT} and I_{LOAD} can be considered equal with sufficient accuracy.

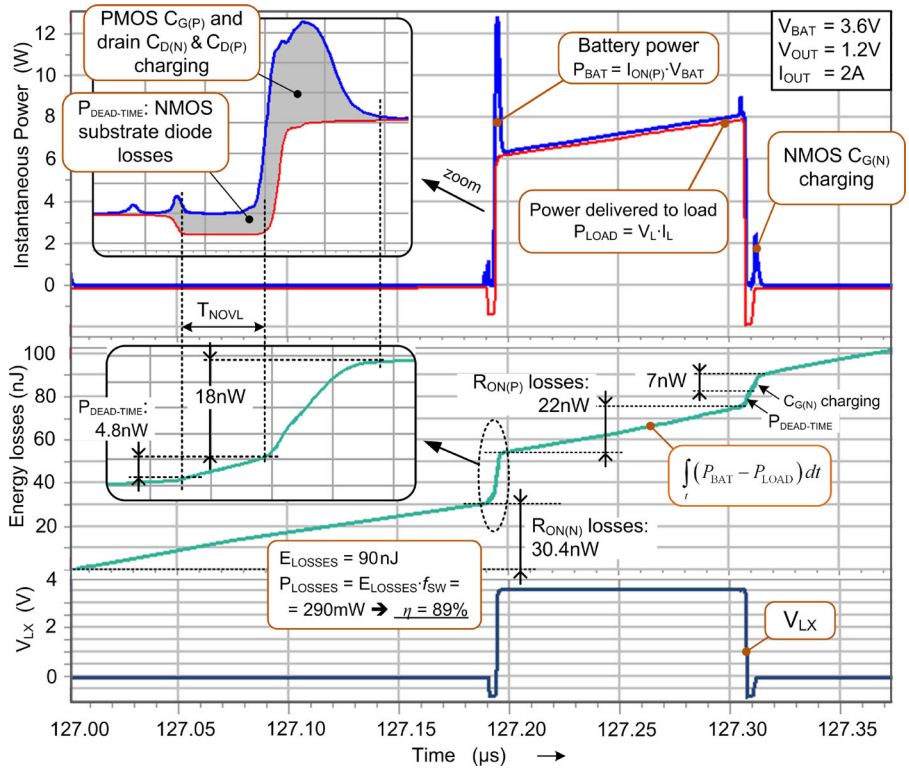

Fig. 4. Representation of the power-lossy contributors from (3).

In order to provide more detailed description, (1) can be extended as the sum of following contributions

$$\begin{aligned} P_{\mathrm{LOSSES}} = & P_{\mathrm{LOSSES}(N)} + P_{\mathrm{LOSSES}(P)} + P_{\mathrm{DEAD-TIME}} + P_{\mathrm{OUT}} \\ & + \underbrace{(1-D)\,R_N I_{\mathrm{OUT}}^2 + C_{G(N)} V_{\mathrm{BAT}}^2 f_{\mathrm{SW}}}_{P_{\mathrm{LOSSES}(N)}} \\ & + \underbrace{\mathrm{DR}_P I_{\mathrm{OUT}}^2 + C_{G(P)} V_{\mathrm{BAT}}^2 f_{\mathrm{SW}}}_{P_{\mathrm{LOSSES}(P)}} \\ & + \underbrace{C_{\mathrm{OUT}} V_{\mathrm{BAT}}^2 f_{\mathrm{SW}}}_{P_{\mathrm{OUT}}} \\ = & \underbrace{\frac{2T_{\mathrm{NOVL}} V_{F(N)} I_{\mathrm{OUT}}}{T_{\mathrm{CLK}}}}_{\mathrm{NMOS\,body-diode\ losses}}. \end{aligned} \tag{3}$$

In this equation, $P_{\mathrm{LOSSES}(N)}$ and $P_{\mathrm{LOSSES}(P)}$ relate to the independent contributions of the NMOS and PMOS power transistors. P_{OUT} relates to the contribution of the output capacitor C_{OUT}, and $P_{\mathrm{DEAD-TIME}}$ to the *dead-time* dependent losses occurring on the forward-biased power transistor body diode. This conduction occurs during the nonoverlapping phases $\mathrm{T_{NOVL}}$ of CMD_P and CMD_N gate signals (see Fig. 4, [10], [14]).

Equation (3) signifies that the power losses are distributed between the NMOS and PMOS power switches. For this reason, independent optimization of the NMOS and PMOS power efficiencies is to be provided.

A detailed representation of the power-loss contributors from (3) is shown in Fig. 4. This figure shows the power P_{BAT} delivered from the battery and power P_{LOAD} delivered to the load. The middle curve corresponds to the time integral of the power losses $(P_{\mathrm{BAT}} - P_{\mathrm{LOAD}})$. In this integral, contributions from (3) are highlighted. Namely, the power dissipation related to the charging of the PMOS gate and C_{LX} capacitances occurs at V_{LX} transition $0 \rightarrow V_{\mathrm{BAT}}$, whereas the dissipation related to the NMOS gate capacitance charging occurs at V_{LX} transition $V_{\mathrm{BAT}} \rightarrow 0$ V. The characteristics was obtained by simulation of the power stage described in Section IV for $V_{\mathrm{BAT}} = 3.6$ V, $V_{\mathrm{OUT}} = 1.2$ V, $I_{\mathrm{OUT}} = 2$ A, R_H, $R_L = 10\,\mathrm{m\Omega}$, $R_{\mathrm{COIL}} = 20\,\mathrm{m\Omega}$ and $R_{\mathrm{PCB,IN}}$, $R_{\mathrm{PCB,OUT}} = 0\,\Omega$. The power stage operates with full NMOS and PMOS sizes. In Fig. 4, the Joule losses dominate over the dynamic losses for both NMOS and PMOS transistors.

In the power stage model shown in Fig. 2, all metallic and coil resistances can be considered constant for one particular power stage and operating temperature range. On the contrary, MOS R_{ON} resistances vary with transistor size W/L, V_{BAT}, and with the statistical and temperature variation of the process constants $K_P = \mu_0 C_{\mathrm{OX}}$ and V_{TH} (gate driving voltage is considered $V_{GS} = V_{\mathrm{BAT}}$)

$$\begin{aligned} R_{\mathrm{ON}(N)} &= \frac{1}{K_{P(N)} \frac{W_N}{L_N} \left(V_{\mathrm{BAT}} - V_{\mathrm{TH}(N)}\right)} \\ R_{\mathrm{ON}(P)} &= \frac{1}{K_{P(P)} \frac{W_P}{L_P} \left(V_{\mathrm{BAT}} - \left|V_{\mathrm{TH}(P)}\right|\right)}. \end{aligned} \tag{4}$$

The gate capacitance of the transistor in an ohmic region depends primarily on the channel surface $W_{(N,P)} \cdot L$, and on the drain and source lateral diffusion areas $2L_D \cdot W_{(N,P)}$ creating the overlap capacitance C_{OV} (L_D is the lateral diffusion length).

This gate capacitance $C_{G(N,P)}$ can be expressed as

$$C_{G(N,P)} \cong C_{\mathrm{OX}} \left(W_{(N,P)} \left(L_{(N,P)} + 2L_D \right) \right). \tag{5}$$

As shown by (3) and Fig. 4, V_{LX} node transition from 0 V to V_{BAT} also introduces power losses caused by the periodical charging of the output capacitance C_{LX}. This capacitor is composed of the parasitic wiring capacitance C_{OUT} in V_{LX} node, and NMOS and PMOS drain capacitances $C_{D(N,P)}$

$$C_{\mathrm{LX}} = C_{\mathrm{OX}} L_D \left(W_N + W_P \right) + C_{\mathrm{OUT}}. \tag{6}$$

It follows, that the MOS drain capacitance contributes twice to the switching losses. Moreover, although the gate capacitance $C_{G(N,P)}$ can be varied by controlling the power-stage size, the drain capacitances of the NMOS and PMOS transistors are hard-connected and are therefore constant.

It is to be mentioned that expressions (5) and (6), are approximate, and neglect the complicated nonlinear behavior below V_T, as well as other parasitic capacitances such as the depletion capacitances C_j of the drain and source PN junctions. However, as shown in following, the nonlinear behavior and other parasitic capacitances are accurately reproduced in the peak-efficiency detection circuit. This important feature facilitates the accurate detection of the peak-efficiency point and allows us to simplify the following mathematical description.

B. Peak-Efficiency Operations

The maximum efficiency point of the switching power stage can be obtained from the derivation of the power efficiency function $\eta = P_{\mathrm{LOAD}}/P_{\mathrm{BAT}}$ as

$$I_{\mathrm{OUT}(\max \eta)} \quad : \quad \frac{d\eta}{dI_{\mathrm{OUT}}} = 0. \tag{7}$$

By using terms from (3), this derivation can be expanded in (8), as shown at the bottom of the page. Solving this derivation yields the peak-efficiency output current $I_{\mathrm{OUT}(\max \eta)}$

$$I_{\mathrm{OUT}(\max \eta)} = V_{\mathrm{BAT}} \sqrt{C \cdot f_{\mathrm{SW}} / (T_{\mathrm{ON}} R)}. \tag{9}$$

As it can be noticed, the power losses $P_{\mathrm{DEAD-TIME}}$ originating from the body-diode conduction do not influence the value of $I_{\mathrm{OUT}(\max \eta)}$ (nevertheless, the dead-time is to be maintained at a small value in order to improve the overall efficiency [10], [11]). This signifies that the peak efficiency occurs when the switching and ohmic losses are equal. This can be expressed by rearranging (9) as

$$R I^2_{\mathrm{OUT}(\max \eta)} = C V^2_{\mathrm{BAT}} f_{\mathrm{SW}}. \tag{10}$$

However, we notice the presence of square terms on both sides, which are difficult to handle by analog circuits.

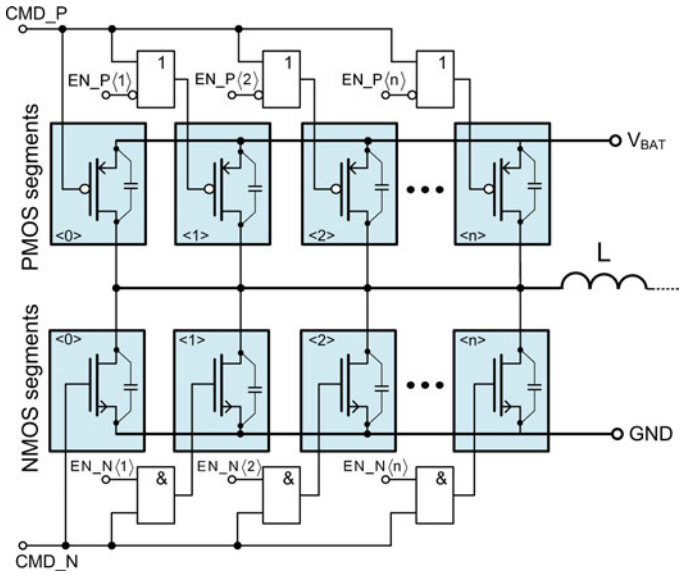

Fig. 5. Simplified representation of the segmented buck converter power stage. The power-MOS segments are controlled by *ENABLE* signals to obtain the tradeoff between the ohmic and dynamic losses.

C. Concept of the Segmented Power Stage

The optimization of the power balance (10) is usually achieved by a careful choice of the NMOS and PMOS power transistors' physical sizes, and choice of the optimal switching frequency f_{SW}. However, the systems based on the segmented (modular) power stage were presented in the literature [3]–[5], and are in the portfolio of some SMPS fabricants [6]. The segmented power stage shown in Fig. 5 allows us to digitally select the active size of the power MOS transistors, in order to establish suitable R_{ON}/C_G tradeoff. As an example, power stage size optimization based on the lookup table is presented in [7]. It is evident, that the use of the lookup table approach involves employment of additional large digital circuit. In this type of approach, the active size of the power stage is usually driven by the output current I_{OUT} or value of the duty-cycle D. Therefore, the lookup table is not able to accurately cover whole space of the dc–dc converter operating conditions, as the chip-by-chip variation of R_{ON}, R_{ON} variation with temperature and V_{BAT}, or variation of dynamic losses with f_{SW}.

The measured example of the power efficiency as a function of the NMOS and PMOS transistor sizes is shown for high and low duty cycle operations in Fig. 6. It can be observed that the optimal sizes of the NMOS and PMOS power transistors are opposite for the low and high duty-cycle values. By the modulation of the power-transistor sizes, the gain of the power-efficiency can reach up to 10% in low and middle current area. In Fig. 6, the maximum efficiency is highlighted and refers to the amount of active NMOS and PMOS segments. As already mentioned, obtaining this maximal efficiency is the goal of the peak-efficiency

$$\frac{d}{dI_{\mathrm{OUT}}} \left\{ \frac{V_{\mathrm{OUT}} \cdot I_{\mathrm{OUT}}}{V_{\mathrm{OUT}} I_{\mathrm{OUT}} + R I^2_{\mathrm{OUT}} + C V^2_{\mathrm{BAT}} f_{\mathrm{SW}} + 2 T_{\mathrm{NOVL}} I_{\mathrm{OUT}} V_{F(N)} / T_{\mathrm{CLK}}} \right\} = 0 \tag{8}$$

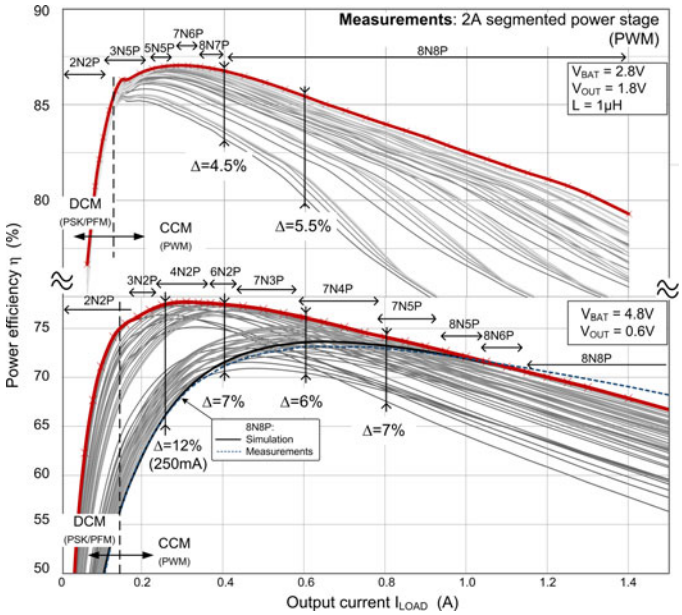

Fig. 6. Measured power-efficiency for 2 A segmented power stage for all combinations of the segments. The labels, e.g., 4N2P signify that 4NMOS and 2PMOS segments were active.

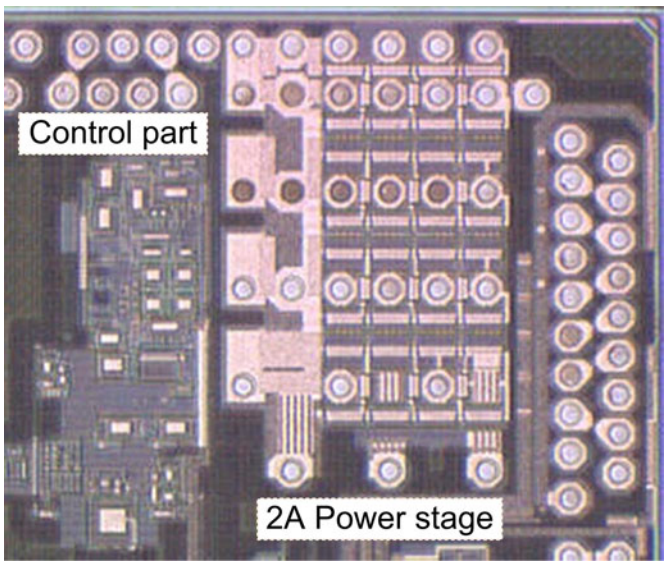

Fig. 7. Photograph of the fabricated 2 A dc–dc converter on 1.3 mm × 1.1 mm surface with Cu-pillar pads. The left side contains the dc–dc converter control part, right side the modular 2-A power stage.

tracking algorithm. Efficiency measurement from Fig. 6 was provided on the integrated 2-A power stage shown in Fig. 7. During the measurement, the integrated converter was mounted in an IC test-socket. Due to high access resistances and parasitic capacitance of this socket, the efficiency exhibits significant several % efficiency drop compared to the standard PCB surface mounting.

Fig. 6 also contains a simulated characteristic for $V_{\mathrm{BAT}} = 4.8$ V and $V_{\mathrm{OUT}} = 0.6$ V 8N8P configuration. This curve allowed us to evaluate the power stage model accuracy, relevant for the following description and validation of the peak-efficiency detection method.

In this paper, method which allows us to detect the peak-efficiency condition (10) of the periodically switching MOS power transistor is presented. The analog "algorithm" developed here takes into account main contributors responsible for the power-losses. As an example of application, the peak-efficiency tracking system is demonstrated on the 5-A buck dc–dc converter designed in 130 nm 5 V, $L_{\mathrm{MIN}} = 0.5\ \mu$m Cu-metal CMOS process. The results presented here are based on the complex simulations of designed and layouted 5 A 3.2-MHz buck dc–dc converter. The model used in the simulation includes an extracted layout and package interconnections, as well as PCB trace resistances.

Although the application example presented here concerns the step-down dc–dc converter, the concept of the peak-efficiency tracking can be generally applied to any switching power MOSFET. For this purpose, circuit of the peak-efficiency detection is to be adapted namely with respect to the position of concerned power switch. For instance, the optimization of the flying power switch in the step-up dc–dc converter can be advantageously based on the bottom power-switch current sensing. The design of the efficiency detection circuit can therefore be entirely referred to GND. Another example can be a high-current charge pump. Here, the optimization can advantageously use the fragmentation pump capacitor, which allows us to account for the dominant bottom-plate dynamic parasitic losses.

The peak-efficiency tracking was initially designed for the four-phase 20-A step-down dc–dc converter intended for future smartphones and tablets ARM application processors.

II. Power-Efficiency Optimization

A. Optimum Operation Point

By manipulating (10), we can obtain approximate optimal operating points for NMOS and PMOS power switches, corresponding to the peak efficiency operations for given $V_{\mathrm{BAT}}, V_{\mathrm{OUT}}$, and f_{SW}. In this first step, we consider only the NMOS transistor with zero access and coil resistances. We also neglect the contribution of the output capacitance C_{LX}, and contribution of the triangular inductor current ΔI_L [i.e., I_{OUT} is considered constant during NMOS conduction as described by (2)]. In this case, (10) can be arranged as

$$(1-D)\,R_{\mathrm{ON}(N)} I^2_{\mathrm{OUT}(\max\eta)} = C_{G(N)} V^2_{\mathrm{BAT}} f_{\mathrm{SW}} \qquad (11)$$

when multiplying both sides by $R_{\mathrm{ON}(N)}$ and applying the square root, we obtain the transistor's V_{DS} average voltage $V_{N\_\mathrm{AVG}(\max\eta)}$, averaged during the whole conduction cycle T_{CLK}

$$\underbrace{(1-D)\,R_{\mathrm{ON}(N)} I_{\mathrm{OUT}(\max\eta)}}_{V_{N\_\mathrm{AVG}_{(\max\eta)}}} = V_{\mathrm{BAT}} \sqrt{(1-D)\,R_{\mathrm{ON}(N)} C_{G(N)} f_{\mathrm{SW}}}. \qquad (12)$$

By averaging the NMOS transistor V_{DS} voltage only during its conduction time $T_{\mathrm{ON}(N)}$, we obtain a $V_{N\_\mathrm{ON\_AVG}(\max\eta)}$

voltage

$$\underbrace{R_{\mathrm{ON}(N)} I_{\mathrm{OUT}(\max \eta)}}_{V_{N\_\mathrm{ON}\_\mathrm{AVG}(\max \eta)}} = V_{\mathrm{BAT}} \sqrt{\frac{R_{\mathrm{ON}(N)} C_{G(N)} f_{\mathrm{SW}}}{(1-D)}}. \quad (13)$$

If this average voltage is measured across the NMOS transistor, the peak-efficiency operation is reached. Indeed, it is simple to obtain the left side of (13) by a current-sensing circuit shown in Section II-C. On the contrary, the value of right side is dependent on the process constant, and its generation is therefore difficult.

B. Optimal V_{DS} Average Voltage

By developing (13) with simple approximations (4) and (5), we can estimate optimal average voltages $V_{N\_\mathrm{ON}\_\mathrm{AVG}(\max \eta)}$ and $V_{P\_\mathrm{ON}\_\mathrm{AVG}(\max \eta)}$ for the NMOS and PMOS power switches

$$V_{N,P\_\mathrm{ON}\_\mathrm{AVG}(\max \eta)} = \frac{V_{\mathrm{BAT}} L_{(N,P)}}{\sqrt{D_{(N,P)}}} \sqrt{\frac{f_{\mathrm{SW}}}{\mu_{(N,P)}}} \sqrt{\frac{1}{V_{\mathrm{BAT}} - |V_{\mathrm{TH}(N,P)}|}} \quad (14)$$

where $D_{(P)} = D$ and $D_{(N)} = (1-D)$. This signifies that the optimum efficiency point primarily depends on the electron or hole mobility $\mu_{(N,P)}$, the switching frequency f_{sw}, the duty-cycle ratio $D_{(N,P)}$, the battery voltage V_{BAT}, and the temperature T. We also notice that this voltage is not dependent on the transistor width $W_{(N,P)}$. This is convenient because it allows us to develop optimization algorithm ideally independent on the channel width of the power transistor.

As an example, optimal $V_{N\_\mathrm{ON}\_\mathrm{AVG}(\max \eta)}$ and $V_{P\_\mathrm{ON}\_\mathrm{AVG}(\max \eta)}$ voltages of NMOS and PMOS power switches result for $V_{\mathrm{BAT}} = 3.6$ V, $L = 0.5$ μm, $f_{\mathrm{sw}} = 3.2$ MHz, $V_{\mathrm{TH}(N,P)} = 0.5$ V, $\mu_N = 207$ cm^2/V·s, and $\mu_P = 85$ cm^2/V·s in:

1) $V_{N\_\mathrm{ON}\_\mathrm{AVG}(\max \eta)} = 12.7$ mV $(D = 0)$;
2) $V_{P\_\mathrm{ON}\_\mathrm{AVG}(\max \eta)} = 20$ mV $(D = 1)$.

Indeed, the algorithm of the power-efficiency optimization can be simplified to the evaluation of the average V_{DS} voltages. On this account, the sensing circuit reproducing the voltage drop on the resistive paths R_N and R_P is now introduced.

C. V_{LX} Masking Circuit

Because the power dissipated on the resistances R_N and R_P is related to the switching times $T_{\mathrm{ON}(N)}$ and $T_{\mathrm{ON}(P)}$ (i.e., times where the respective switches are ON), V_{LX} off-state voltage masking circuit can be used to help extract:

1) average voltage $V_{N\_\mathrm{SWITCHON}\_\mathrm{AVG}}$ and $V_{P\_\mathrm{SWITCHON}\_\mathrm{AVG}}$ appearing across the switch resistances $(R_{N\_\mathrm{SWITCH}}, R_{P\_\mathrm{SWITCH}})$ during the MOS conduction phases $T_{\mathrm{ON}(N)}$ or $T_{\mathrm{ON}(P)}$;
2) average voltages $V_{N\_\mathrm{ON}\_\mathrm{AVG}}$ and $V_{P\_\mathrm{ON}\_\mathrm{AVG}}$ appearing across the parasitic resistances R_N and R_P of $I_{\mathrm{ON}(N)}$ and $I_{\mathrm{ON}(P)}$ current paths during the MOS conduction phases $T_{\mathrm{ON}(N)}$ or $T_{\mathrm{ON}(P)}$.

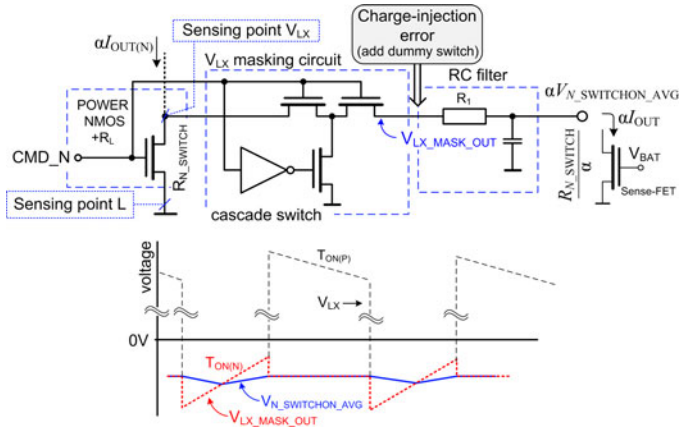

Fig. 8. V_{LX} off-state voltage masking circuit for NMOS power transistor and related time diagram; dummy switch is used to prevent the output $V_{\mathrm{LX\_MASK\_OUT}}$ node from the charge-injection error.

For this purpose, V_{LX}-masking circuit helps to remove the unnecessary high voltage across NMOS or PMOS switches appearing when these switches are nonconducting.

In the following, example of the V_{LX} voltage masking current-sensing circuit will be shown on the bottom NMOS transistor (see Fig. 2). For the upper PMOS transistor (can also be a NMOS when dual-N structure is used), the V_{LX}-masking circuit is identical, except that the voltage inverter is replaced by the voltage follower.

D. I_{OUT} Current Sensing by V_{LX} Masking Circuit

For the purpose of power-efficiency detection, measurement of the output current I_{OUT} is required. This allows us to reproduce the α-scaled Joule losses dissipated on the resistive elements R_N and R_P of the $I_{\mathrm{ON}(N)}$ or $I_{\mathrm{ON}(P)}$ current paths.

In fact, any current-sensing circuit able to generate the absolute value image αI_{OUT} of the output current can be utilized. For instance, [12] describes an accurate current sensing circuit for the buck dc–dc converter power stage. The silicon implementation of this technique proved few% accuracy and very-high linearity. Less accurate, but simpler solution can be based on the V_{LX} masking circuit, also described in [12] and shown in Fig. 8.

During the conduction phase $T_{\mathrm{ON}(N)}$, the V_{LX} masking circuit generates the output voltage $V_{\mathrm{LX\_MASK\_OUT}} = R_{N\_\mathrm{SWITCH}} \cdot I_{\mathrm{OUT}}$. In the remaining time, the output is set to high impedance. Thanks to this, an *RC* filter averages the voltage $V_{\mathrm{LX\_MASK\_OUT}}$ during the transistor conduction, and holds the average voltage on the filter capacitor afterward. The obtained output voltage is labeled as $V_{N\_\mathrm{SWITCHON}\_\mathrm{AVG}}$.

The V_{LX}-masking circuit is implemented as the serial cascade switch, in order to sufficiently filter the negative V_{LX} voltage during the NMOS transistor's body-diode conduction and V_{LX} voltage ringing.

By applying the $V_{N\_\mathrm{SWITCHON}\_\mathrm{AVG}}$ to the α-scaled sense-FET also including scaled parasitic resistance $R_{N\_\mathrm{SWITCH}}/\alpha$, an absolute value continuous image αI_{OUT} of the output current I_{OUT} is obtained. (i.e., value with known α and without

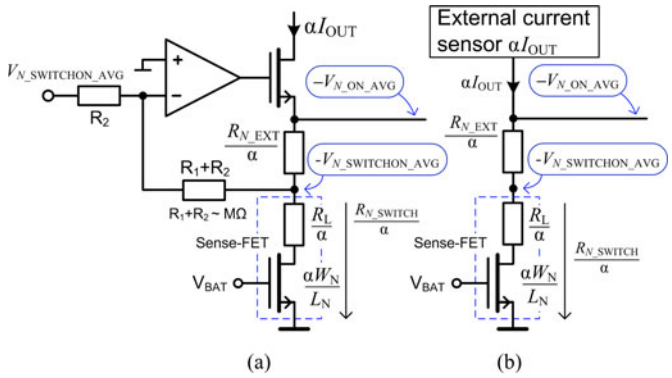

Fig. 9. Implementation of the circuit allowing to reconstitute the image of the Joule losses appearing on the resistance R_N of the $I_{\mathrm{ON}(N)}$ current path. Solution (a) is intended for the use with V_{LX}-masking circuit from Fig. 8, and solution (b) for the use with an external (more accurate) current sensor, e.g., [12].

duty-cycle dependence—see [13] for more details). By analyzing the circuit from Fig. 8, the average output voltage $V_{N\_\mathrm{SWITCHON\_AVG}}$ can be written as

$$V_{N\_\mathrm{SWITCHON\_AVG}} = R_{N\_\mathrm{SWITCH}} I_{\mathrm{OUT}}. \tag{15}$$

The relation between powers dissipated on the power MOS and on the sense-FET transistors can be then derived as

$$P_{\mathrm{SENSE\_FET}} = \alpha^2 I_{\mathrm{OUT}}^2 \frac{R_{N\_\mathrm{SWITCH}}}{\alpha\,(1-D)} = \alpha \frac{P_{N\_\mathrm{SWITCH}}}{1-D}. \tag{16}$$

As already mentioned, the current αI_{OUT} passing through the sense-FET is the absolute-value image of the output current, i.e., has no duty-cycle dependence. Therefore, by applying this replica current αI_{out} to resistance R_N/α, voltage drop related to the *total Joule losses* occurring during the NMOS conduction phase $T_{\mathrm{ON}(N)}$ can be reconstituted. This voltage is

$$V_{N\_\mathrm{ON\_AVG}} = I_{\mathrm{OUT}} R_N. \tag{17}$$

The total Joule losses occurring during the steady-state operation of the dc–dc converter are therefore referred by (1-D) ratio

$$P_N = (1-D)\, R_N I_{\mathrm{OUT}}^2. \tag{18}$$

A circuit allowing us to obtain $V_{N\_\mathrm{ON\_AVG}}$, and to generate the image of the output-current αI_{OUT} can be based on the realizations shown in Fig. 9.

As we can see, the solution (a) is intended for the use with V_{LX}-masking circuit from Fig. 8, whereas solution (b) is intended for the use with an external more accurate current sensor (for instance solution [12]). The voltage inverter in solution (a) is used because $V_{N\_\mathrm{SWITCHON\_AVG}}$ of the bottom NMOS switch is negative for $I_{\mathrm{LOAD}} > 0$. For the PMOS (upper switch) variant, a voltage follower is to be used, as the $V_{P\_\mathrm{SWITCHON\_AVG}}$ value is always below V_{DD} for $I_{\mathrm{LOAD}} > 0$. However, in order to provide the simplification of the design and to reduce the circuit's power consumption, single V_{LX}-masking circuit can be integrated. The output current image αI_{OUT} can be then shared between the peak-efficiency detection circuits of the NMOS and PMOS power transistors.

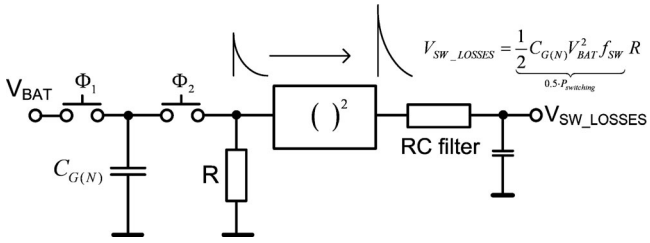

Fig. 10. Implementation of circuit for the switching losses measuring.

III. Circuit for Peak-Efficiency Detection

A. Dynamic Losses Measurement

The charging and discharging of the gate capacitance is a very fast process. Therefore, rather than provide direct measurements of the fast dynamic switching current, slow measurement of the power stored in the charged capacitor may be preferred. This can be done by a system periodically discharging the capacitor into a resistance. An example of the system measuring the energy accumulated in a capacitor is shown in Fig. 10. Here, we can see that the energy stored in the charged capacitor during the first (accumulation) phase Φ_1 will be dissipated during the second phase Φ_2 (ideally at $t \to \infty$) at resistance R. As shown in Fig. 10, obtained dc voltage $V_{\mathrm{SW\_LOSSES}}$ is directly related to the energy required for the periodical charging of the gate capacitance $C_{G(N)}$. By handling this voltage, the equilibrium between switching and joule losses can be found mathematically.

However, realization of the fast quadratic term can decrease the reliability and increase the complexity of the circuit, and is therefore not convenient. Nevertheless, the slow energy transfer between capacitive and resistive lossy elements is a base of the presented method.

B. RC Energy Balancing Circuit

The method of the peak efficiency detection relies on a circuit that allows us to transfer the amount of energy dissipated on the parasitic resistance R_N to an auxiliary capacitor $C'_{G(N)} = C_{G(N)}$. When energy required to charge the capacitor $C_{G(N)}$ and energy corresponding to the joule heat dissipated on R_N during one conduction cycle are equal, the capacitor $C'_{G(N)}$ will be charged exactly to V_{BAT}. The voltage across $C'_{G(N)}$ therefore provides information about the peak-efficiency operations. Said otherwise, in the case of peak-efficiency operation, auxiliary capacitor stores identical amount of the energy as the energy being dissipated on the resistance R_N during one conduction cycle.

The methodology introduced here is demonstrated on the NMOS part of the power switch. However, as shown by (3), two circuits allowing independent peak-efficiency detection of the bottom NMOS and upper NMOS or PMOS power switches are to be implemented in the case of the buck-converter power stage.

The principle of the method relies on the definition of the work required to establish a voltage V across the capacitor

plates. This work can be developed as

$$W = \int_0^Q V dq = \int_0^Q \frac{q}{C} dq = \frac{1}{2} C V^2 = \frac{1}{2} V Q. \tag{19}$$

From physical definition, electrical charge Q can also be expressed as the current by time product $I_B \cdot t$. On this account, the last term in (19) can be written in following form:

$$W = \frac{1}{2} V_{\mathrm{BAT}} Q = \frac{1}{2} V_{\mathrm{BAT}} I_B T_{\mathrm{CLK}} \tag{20}$$

where I_B is constant bias current which is to be applied to the auxiliary capacitor $C'_{G(N)}$. However, this equation is only valid when $I_B T_{\mathrm{CLK}} = C \cdot V_{\mathrm{BAT}}$. For this particular value of I_B, voltage V_{BAT} across the capacitor is obtained at $t = T_{\mathrm{CLK}}$.

In the process of capacitor charging, exactly one half of the energy is dissipated on buffer resistance, and one half is stored in the capacitor. On this account, term $\frac{1}{2}$ in (20) disappears. Now, (10) can be written as combination of (18) and (20), resulting in the energy balance

$$(1 - D)\, R_N I_{\mathrm{OUT}}^2 = I_B T_{\mathrm{CLK}} V_{\mathrm{BAT}} f_{\mathrm{SW}}. \tag{21}$$

This allows us to obtain the value of I_B which is to be integrated by $C'_{G(N)}$

$$I_B = (1 - D)\, I_{\mathrm{OUT}}^2 \frac{R_N}{V_{\mathrm{BAT}}}. \tag{22}$$

By rearranging this (22), we can obtain the bias current value as

$$I_B = (1 - D)\, \underbrace{I_{\mathrm{OUT}} R_N}_{V_{N\_\mathrm{ON\_AVG}}} \cdot \underbrace{\frac{I_{\mathrm{OUT}}}{V_{\mathrm{BAT}}}}_{1/R_X} \tag{23}$$

where $(1-D)$ is the relative conduction time for the NMOS transistor (i.e., become D for PMOS transistor). This equation presents the most important conclusion of the study. In fact, (23) allows us to realize analog circuit which further allows us to measure the average energy dissipated on the resistance R_N during one clock period, and to store the identical amount of the energy into the auxiliary capacitor $C'_{G(N)}$. If the voltage V_{CAP} integrated on the capacitor $C'_{G(N)}$ is exactly V_{BAT} at the end of integration interval T_{CLK} (i.e., $V_{\mathrm{CAP}(t=T_{\mathrm{CLK}})} = V_{\mathrm{BAT}}$), the peak-efficiency operation is reached. Otherwise, if $V_{\mathrm{CAP}(t=T_{\mathrm{CLK}})}$ voltage is lower than V_{BAT}, the capacitive dynamic losses dominate (power-MOS size is to be decreased), and on the contrary, when $V_{\mathrm{CAP}(t=T_{\mathrm{CLK}})}$ reaches the battery voltage before $t = T_{\mathrm{CLK}}$, the ohmic losses dominate and the power MOS size is to be increased.

C. Circuit Implementation

By replacing T_{CLK} in (20) by $T_{\mathrm{ON(N)}} = (1\text{–}D) \cdot T_{\mathrm{CLK}}$, (21) can be simplified to

$$R_N I_{\mathrm{OUT}}^2 = I_B T_{\mathrm{ON}(N)} V_{\mathrm{BAT}} f_{\mathrm{SW}}. \tag{24}$$

This means that the integration time (i.e., time when $C'_{G(N)}$ is charged by I_B) decreases. This time is now equal to the conduction time of the power switch: $D \cdot T_{\mathrm{CLK}}$ for PMOS and $(1-D) \cdot T_{\mathrm{CLK}}$ for NMOS. This allows us to obtain the integration current in the following form:

$$I_B = \underbrace{I_{\mathrm{OUT}} R_N}_{V_{N\_\mathrm{ON\_AVG}}} \cdot \underbrace{\frac{I_{\mathrm{OUT}}}{V_{\mathrm{BAT}}}}_{1/R_X}. \tag{25}$$

In this equation, the term $V_{N\_\mathrm{ON\_AVG}}$ corresponds to the voltage obtained by the circuit shown in Fig. 9.

In order to realize the circuit operating with microampere currents, and in order to enable the realization of linear variable resistance R_X, current I_{OUT} and voltage V_{BAT} across R_X are to be decreased. The constant α and β are therefore introduced to (25)

$$I_B = \underbrace{I_{\mathrm{OUT}} R_N}_{V_{N\_\mathrm{ON\_AVG}}} \cdot \underbrace{\frac{\alpha I_{\mathrm{OUT}}}{\beta V_{\mathrm{BAT}}}}_{1/R_X}. \tag{26}$$

For instance, $\alpha = 25 \times 10^{-6}$ and $\beta = 0.01$. By applying this current and voltage scaling, the integration capacitor is to be reduced to $C'_{G(P,N)} = \frac{\alpha}{\beta} C_{G(P,N)}$. Again, if the current I_B is applied to $C'_{G(N)} = \frac{\alpha}{\beta} C_{G(N)}$, the voltage V_{CAP} reaching V_{BAT} at the end of integration interval signifies that the power switch operates at peak efficiency.

An important feature of this peak-efficiency detection technique is that the scaled capacitor $C'_{G(N)} = \frac{\alpha}{\beta} C_{G(N)}$ is made of the NMOS transistor (similarly, $C'_{G(P)} = \frac{\alpha}{\beta} C_{G(P)}$ of the PMOS transistor). Therefore, nonlinearity and principal parasitic capacitances of the power-NMOS transistor which has been neglected in (5) are accurately reproduced by $C'_{G(N)}$.

Indeed, (26) can be implemented by an analog circuit realized in CMOS process. The circuit for the peak-efficiency detection of the periodically switching power MOS transistor performs the following operations:

1) obtains the scaled replica of the output current αI_{OUT};
2) creates the auxiliary resistance $R_X = \beta \cdot V_{\mathrm{BAT}} / \alpha I_{\mathrm{OUT}}$;
3) recopies the resistance R_X to R'_X;,
4) measures the voltage $V_{N\_\mathrm{ON\_AVG}}$ corresponding to the voltage drop on R_N parasitic resistance;
5) apply $V_{N\_\mathrm{ON\_AVG}}$ to recopied resistance R'_X,;
6) apply the current passing through recopied resistance R_X to discharged auxiliary MOS capacitor $C'_{\mathrm{GS}} = \left(\frac{\alpha}{\beta}\right) C_{\mathrm{GS}}$ during the time equal to the conduction time of related power switch (NMOS or PMOS);
7) observe the voltage V_{CAP} integrated on C'_{GS} at the end of integration interval. If lower than V_{BAT}, the switching losses dominate. If higher, the dominant losses are due to the resistive Joule heat.

Described system can be realized by following schematic Fig. 11. In this schematic, the V_{LX} masking circuit is connected to an inverting amplifier with a gain of -1, as shown in Fig. 9(a). This connection allows us to convert the negative voltage $V_{N\_\mathrm{SWITCHON\_AVG}}$ present across the NMOS switch in the case of positive output current I_{OUT} to the positive value $-V_{N\_\mathrm{SWITCHON\_AVG}}$. However, as the voltage inverter has

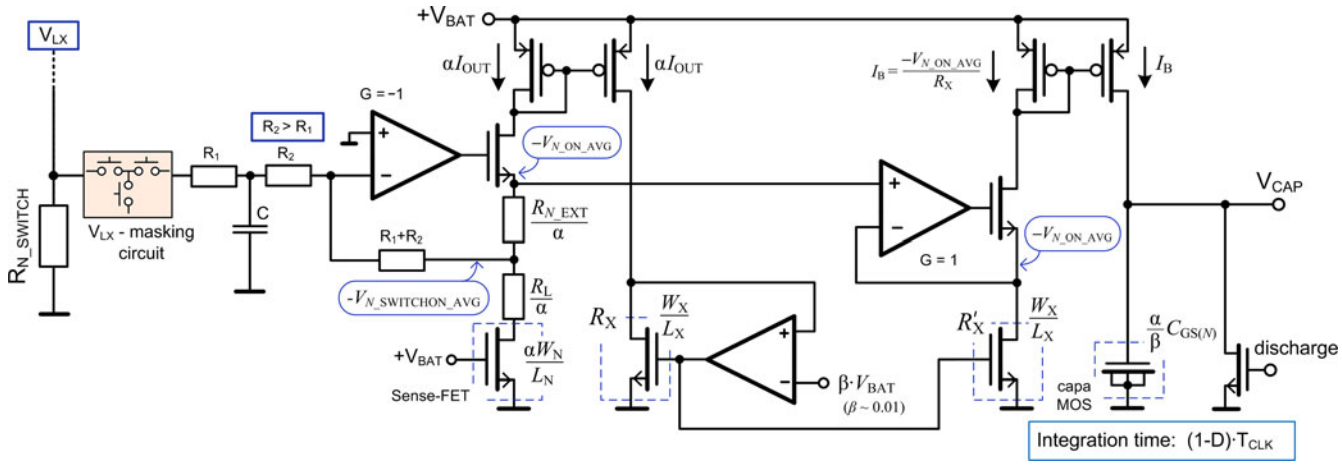

Fig. 11. Circuit of the peak efficiency detection. Modification for the upper power-switch is identical with exception, that the voltage inverter is replaced by the voltage follower. The MOS capacitor is of NMOS or PMOS type, depending on the power-MOS channel type.

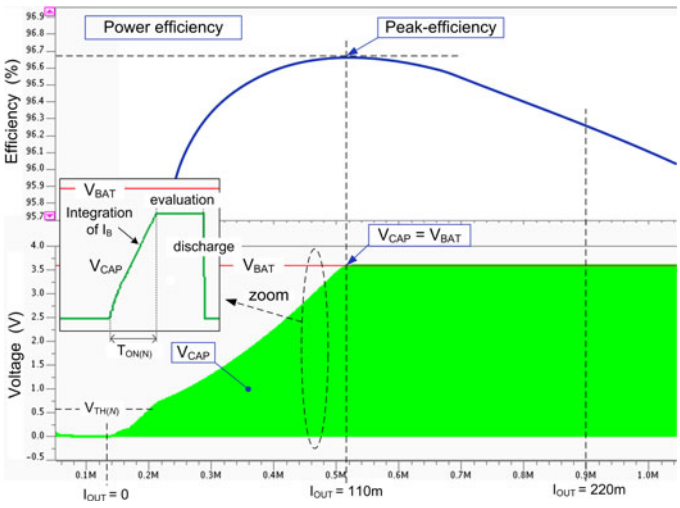

Fig. 12. Simulation of the peak-efficiency detector from Fig. 11. Simulation is done with real NMOS power switch and lossless PMOS switch. V_{CAP} reaches the V_{BAT} at the peak efficiency point.

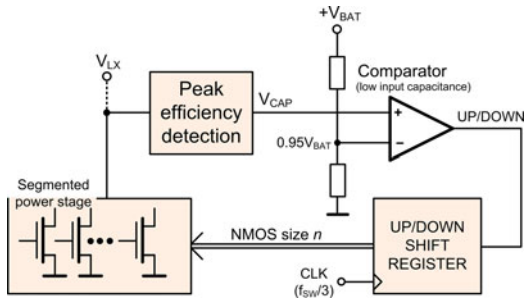

Fig. 13. Block schematic of the peak-efficiency tracking control loop for the NMOS power transistor. In the steady state, the amount of the active power stage segments can oscillate between two neighbors' values.

finite input impedance, condition of $R_2 >> R_1$ should be accomplished. This allows us to protect the capacitor C against the discharge through the operational amplifier virtual zero, when the power NMOS switch is OFF. As already mentioned, unitary voltage follower is used for the upper NMOS/PMOS switch peak-efficiency detector, because $V_{N\_\mathrm{SWITCHON\_AVG}}$ is always below V_{BAT} for positive I_{OUT}.

Concerning the implementation of R_X and R'_X, good matching between both transistors should be provided. In the CMOS integration presented in Section IV-D, part of R_X value was obtained by the metallic resistance. This allowed us to improve the accuracy of R'_X thanks to a good resistor matching in the CMOS process.

The demonstration of the peak-efficiency detection circuit operation is shown here by the simulation on Fig. 12. This simulation was done with real (lossy) NMOS and ideal (lossless) PMOS power switch models. This allows us to trance the power efficiency of the NMOS part of the power stage only. By linear sweep of the output current from 0 to 300 mA, the auxiliary capacitor voltage V_{CAP} reaches V_{BAT} at the point of maximum efficiency.

In the zoomed detail of V_{CAP}, three phases of the detector's operations can be identified: 1) Integration of the current I_B by $C'_{G(N)}$, 2) evaluation, when the capacitor holds the integrated voltage value and comparator detect if V_{CAP} approached V_{BAT} or not, and 3) capacitor reset phase. All these phases are driven by internal control logic.

IV. Peak-Efficiency Tracking Algorithm

As mentioned in the introduction, the optimization of step-down dc–dc converter conversion efficiency is done by the independent control of the power NMOS and PMOS channel widths. Alternatively, the modulation of the switching frequency f_{SW} or the power-MOS gate voltage V_{GS} can also be envisaged [8], [9].

The concept of the peak-efficiency tracking developed here is based on the *on-the-fly* adjustment of the segmented power-stage PMOS and NMOS sizes: when the peak-efficiency detection shows that the switching-losses are dominating, the power-stage sizes decrease and vice versa (see Section I-C).

Beside the segmented power stage, the peak-efficiency tracking feature requires integration of a simple iterative control loop shown in Fig. 13. This control loop contains a comparator,

TABLE I
PARTITIONING AND PARAMETERS OF THE POWER STAGE NMOS PART (PARTITIONING OF PMOS PART IS IDENTICAL)

Segments[1] (n)	α ×10^{-6}	$\mathbf{R_N}$[2] (mΩ)	$\mathbf{P_{JOULE(N)}}$[3] (mW)	$\mathbf{R_L/\alpha}$[4] (Ω)	$\mathbf{R_{N\_EXT}/\alpha}$[4] (Ω)	$\mathbf{W(C_G)}$[5] (μm)	$\mathbf{W(C_{D(N)})}$[6] (μm)	$\mathbf{P_{G(N)}}$[7] (mW)	$\mathbf{P_{CD(N)}}$[8] (mW)	$\mathbf{P_{DYNAMIC(N)}}$[9] (mW)
4	25	86	14.9	400	800	35120	439	2.7	4.3	7.0
5	20	75	12.8	500	1000	43900	351	3.4	4.3	7.7
6	16.7	67	11.5	600	1200	52680	293	4.1	4.3	8.4
7[10]	**14.3**	**62**	**10.6**	**700**	**1400**	**61460**	**251**	**4.7**	**4.3**	**9.1**
9[10]	**11.1**	**55**	**9.63**	**900**	**1800**	**79020**	**195**	**6.1**	**4.3**	**10.4**
12	8.33	48	8.5	1200	2400	105360	146	8.1	4.3	12.4
16	6.25	44	7.7	1600	3200	140480	110	10.8	4.3	15.1
20	5.00	41	6.9	2000	4000	175600	88	13.6	4.3	17.9

Parameters Were Extracted From Simulation for: $V_{BAT} = 3.6$V, $V_{OUT} = 1.2$V, $I_{OUT} = 0.5$A, and $\beta = 0.01$. Parasitic Resistances Were Considered $R_H = R_L = 10$mΩ, $R_{COIL} = 20$mΩ and $R_{PCB,IN} = R_{PCB,OUT} = 0$Ω.

(1) One segment is based on the 8.78mm/0.5μm NMOS transistor, $R_{ON} = 221$mΩ (PMOS segment W/L is 20.74mm/0.5μ).

(2) total resistance of the $I_{ON(N)}$ conduction path.

(3) total ohmic power dissipated during one conduction cycle $T_{CLK} = 312.5$ns.

(4) value of scaled resistances R_L, R_{N_EXT} (Fig. 3).

(5) channel width $W(C_G)$ of the active power-NMOS part.

(6) channel width $W(C_D)$ of the transistor emulation the drain capacitance (Fig. 15).

(7) power $P_{G(N)}$ required to charge the active NMOS gates.

(8) power required to charge all NMOS drain capacitances.

(9) total dynamic power-losses $P_G + P_{CD}$.

(10) Optimal configuration for this operation point.

synchronous up/down shift-register, and the interface allowing us to control the amount of the active power stage segments.

In Fig. 13, the output V_{CAP} of the peak-efficiency detection circuit enters into a low input capacitance comparator. The reference value for this comparator is set close to V_{BAT}, e.g., $0.95{\cdot}V_{BAT}$. This is because of the limited dynamic of the I_B current source. One iteration (i.e., time where the power efficiency is evaluated) was set to three clock cycles. This ensures good stability of the power stage size regulation.

In this paper, the detailed description of the peak-efficiency tracking algorithm implementation is provided with emphasis on the design aspect allowing us to reach high optimization gain.

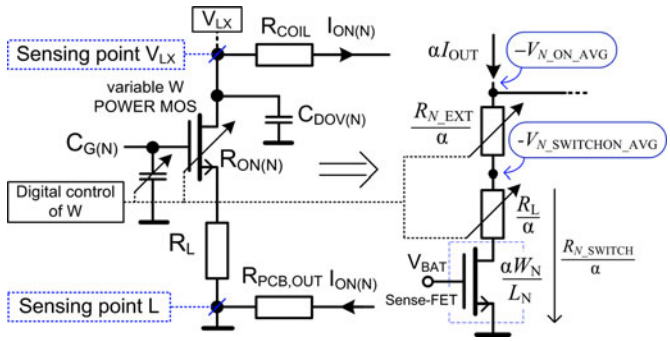

Fig. 14. Scaling of the sense resistances R_{N_EXT} and R_L.

A. 5A Power Stage Partitioning

The 5A segmented power stage is implemented by using the concept shown in Fig. 5. The size of the power stage can be adjusted in 64 steps: eight steps for NMOS part and eight steps for PMOS part. The details concerning the NMOS part partitioning are listed in Table I.

The values mentioned in Table I were obtained by simulation for $V_{BAT} = 3.6$ V, $V_{OUT} = 1.2$ V and $I_{OUT} = 0.5$ A. Parasitic resistances were considered R_H, $R_L = 10$ mΩ, $R_{COIL} = 20$ mΩ and $R_{PCB,IN}$, $R_{PCB,OUT} = 0$ Ω. This table demonstrates the evolution of the joule and dynamic losses $P_{JOULE(N)}$ and $P_{DYNAMIC(N)}$ in function of the power stage active size n. For instance, equilibrium between $P_{JOULE(N)}$ and $P_{DYNAMIC(N)}$ is placed between seven and nine active segments. Others values shown in Table I aim to simplify the description of R_{N_EXT} an R_L resistance scaling, as well as the drain-capacitance $C_{D(N)}$ scaling presented in following sections.

B. Sense-FET, R_{N_EXT} and R_L Resistances Scaling

The scaling-constant α is defined as the ratio between the channel widths of active-part of the power-MOS and sense-FET transistors (channel lengths are identical for both transistors in order to obtain the best possible matching)

$$\alpha = \frac{W_{SENSE-FET}}{W_{POWER-MOS}}. \tag{27}$$

In the implementation, the layout based on the serial-fingers structure [12] was used in order to increase the sense-FET area and thus allowing to improve the matching. As results from (27), the change of the active segments amount n (i.e., $W_{POWER-MOS}$ value) also changes the value of the scaling constant α (see Table I).

As shown in Fig. 14, variation of the power-MOS size $W_{POWER-MOS}$ impacts the value of $R_{ON(N)}$. On the contrary, the values of other parasitic resistances remain unchanged (*note*:

access metallic resistance R_L inside the package can also vary with n, depending on the layout strategy). However, as shown by schematics Fig. 9, the integration of resistances $R_{N\_\mathrm{EXT}}/\alpha$ and R_L/α is required. On this account, the variable resistances should be implemented as suggested in Fig. 14 and shown in Table I.

By using the implementation shown in Fig. 14, accurate current replica αI_{OUT} and in consequence accurate generation of $V_{N\_\mathrm{ON\_AVG}}$ voltage can be obtained. As an example of the resistance scaling, we consider factor $\alpha_1 = 25 \times 10^{-6}$ switched to $\alpha_2 = 12.5 \times 10^{-6}$ (i.e., power MOS channel width $W_{\mathrm{POWER\_MOS}}$ increased by 2). It is found that for the identical current $I_{\mathrm{ON}(N)}$, the voltage drop across the power-MOS R_{ON} is divided by 2. However, the voltage drop across the parasitic resistances $R_{N\_\mathrm{EXT}}+R_L$ remains unchanged. Therefore, the values of the sense resistances R_L/α_2 and $R_{N\_\mathrm{EXT}}/\alpha_2$ are multiplied by 2 compared to R_L/α_1 and $R_{N\_\mathrm{EXT}}/\alpha_1$. For this purpose, the circuit level implementation of Fig. 14 contains one (constant-size) serial-finger [12] sense-FET with $\alpha W_N/L_N = 0.877\ \mu$m/0.5 μm, and banc of R_L/α_n and $R_{N\_\mathrm{EXT}}/\alpha_n$ corresponding to the discrete values n (see Table I).

As already mentioned, serial fingers sense-FET structure [12] is used, in order to increase the effective area $W \cdot L$. By using the four-serial-finger structure, the total area of the sense-FET transistor is increased by 4^2 to $4 \times (4 \times 0.877\ \mu\mathrm{m}) \times 0.5\ \mu$m. Following Pelgrom's rule, the matching between the power-stage and sense-FET is therefore improved approximately four times, compared to a single $\alpha W_N/L_N = 0.877\ \mu$m/0.5 μm sense FET transistor. This matching improvement results in improvements of αI_{OUT} accuracy.

Note: alternative configuration varying the W/L of the sense-FET and keeping constant R_L/α and $R_{N\_\mathrm{EXT}}/\alpha$ resistances can also be used.

C. Power MOS Drain Capacitance

In the segmented power stage shown in Fig. 5, all active and nonswitching power transistors exhibit a nonnegligible drain capacitance $C_{D(N)}$ or $C_{D(P)}$. Their values mainly result from the diffusion (overlap) length L_D and junction capacitance C_j, and were previously expressed as (C_j is neglected here)

$$C_{D(N,P)} = C_{\mathrm{OX}} L_D W_{(N,P)}. \tag{28}$$

In (28), $W_{(N,P)}$ is the total channel width of the power NMOS or PMOS transistors connected to the V_{LX} node (20 segments in our case). As example for $L = 0.5\ \mu$m 5 V power-MOS used in the design presented here, drain capacitance corresponds approximately to 20% of the channel capacitance $C_{\mathrm{OX}} W \cdot L$. This drain capacitance is hard-connected to V_{LX}-node and does not depend on the amount n of the active segments. Therefore, losses $P_{\mathrm{CD}(N)}$ generated by V_{LX} voltage switching are approximately constant—independent on the active power—MOS size $W_{\mathrm{POWER-MOS}}$. When a small size of the power stage is activated, losses $P_{\mathrm{CD}(N)}$ can even be dominating compared to the gate driving power $P_{G(N)}$, (see Table I). Indeed, this restricts the reasonable minimal/maximal power-MOS channel width ratio $W_{\mathrm{POWER-MOS(min)}}/W_{\mathrm{POWER-MOS(max)}}$ to approximately

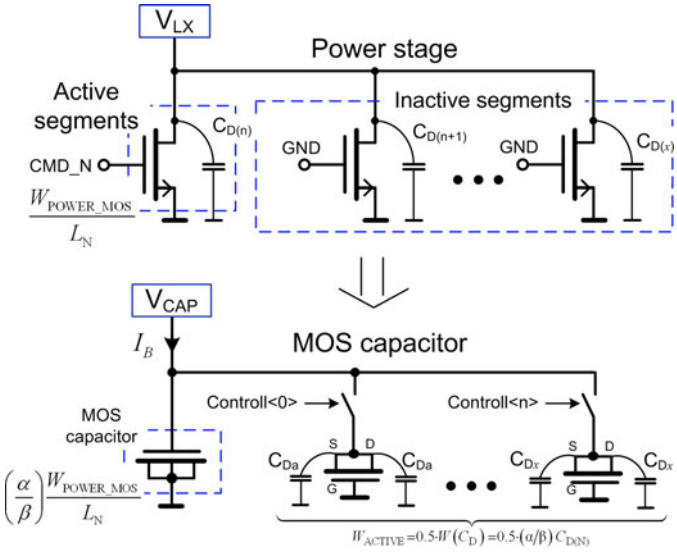

Fig. 15. Emulation of the drain capacitance of inactive nonswitching segments. If the transistor structure is symmetrical, the drain parasitic capacitance is emulated by both drain and source terminals.

25%. On the contrary, if the power stage operates with full-size, the losses created by the V_{LX}-switching can be neglected. In order to include the $P_{\mathrm{CD}(N)}$ and $P_{\mathrm{CD}(P)}$ losses in the peak-efficiency tracking algorithm, the drain parasitic capacitances $C_{D(N)}$ and $C_{D(P)}$ are included in $P_{\mathrm{LOSSES}(N)}$ and $P_{\mathrm{LOSSES}(P)}$ terms of (3) as

$$P_{\mathrm{LOSSES}} = \underbrace{(1-D)\, R_N I_{\mathrm{OUT}}^2 + \left(C_{G(N)} + C_{D(N)}\right) V_{\mathrm{BAT}}^2 f_{\mathrm{SW}}}_{P_{\mathrm{LOSSES}(N)}} + \underbrace{\mathrm{DR}_P I_{\mathrm{OUT}}^2 + \left(C_{G(P)} + C_{D(P)}\right) V_{\mathrm{BAT}}^2 f_{\mathrm{SW}}}_{P_{\mathrm{LOSSES(P)}}}. \tag{29}$$

It follows that the integrating capacitor $C'_{G(N,P)}$ in the peak-efficiency detection circuit is to be increased by $(\alpha/\beta)\, C_{D(N,P)}$, or

$$C'_{G(N,P)} = \frac{\alpha}{\beta}\left(C_{G(N,P)} + C_{D(N,P)}\right) \tag{30}$$

where $C_{G(N)}$ or $C_{G(P)}$ are the sum of gate capacitances of NMOS or PMOS active segments. This signifies that in the peak-efficiency detection circuit, the values of $C'_{G(N)}$ and $C'_{G(P)}$ are to be updated dynamically with the power-stage size, similarly as the R_L/α and $R_{N\_\mathrm{EXT}}/\alpha$ resistances scaling shown in previous section. This dynamic updating is schematically shown for $C'_{G(N)}$ in Fig. 15 and is also listed in Table I.

The demonstration of the dynamical $C'_{G(N)}$ scaling is shown here on an example of the power stage with $n = 4$ active NMOS transistor segments (channel W of one segment = 8780 μm), and 16 inactive segments (i.e. 1st row in Table I). The channel width of the auxiliary capacitor $C'_{G(N)}$ is $4 \cdot \frac{\alpha}{\beta} 8780\ \mu\mathrm{m} = 87.8\ \mu$m ($\alpha = 25 \times 10^{-6}$, $\beta = 0.01$, $L = 0.5\ \mu$m). This auxiliary capacitor $C'_{G(N)}$ already reproduces all parasitic capacitances and nonlinearities of the gate capacitance, as discussed at the end of Section

I-A. However, during the $V_{\rm LX}$ transition 0 V $\rightarrow V_{\rm BAT}$, all 20 segments' drain capacitances are charged. This signifies that the scaled "image" of $C_{D(N)}$ is to be added to the auxiliary capacitor $C'_{G(N)}$. The scaled "image" of $C_{D(N)}$ can be created by a drain terminal of a $W(C_{D(N)}) = 20 \cdot (\alpha/\beta) \cdot 8780\ \mu\text{m} = 439\ \mu\text{m}$ transistor biased in the cut-off regime. In the second example with seven active segments (fourth row in Table I), the channel width of $C'_{G(N)}$ remains unchanged (i.e., $7 \cdot \frac{\alpha}{\beta} 8780\ \mu\text{m} = 87.8\ \mu\text{m}$ for $\alpha = 14.3 \times 10^{-6}$), but overlap capacitance will now be emulated by the $W(C_{D(N)}) = 20 \cdot \frac{\alpha}{\beta} 8780\ \mu\text{m} = 250\ \mu\text{m}$ transistor, because the constant α has changed.

An accurate way to emulate the overlap and junction capacitance is to use the drain terminal of an NMOS or PMOS transistor (depending on the power transistor type), operating in cut-off regime (i.e. with grounded gate and source terminals). In this case, the drain terminal exhibits the required value of the drain capacitance $\left(\frac{\alpha}{\beta}\right) C_{D(N)}$. If the transistor structure is electrically symmetrical, the drain and source exhibit almost identical capacitance. Therefore, in order to decrease the silicon surface, the (D) and (S) terminals can be connected. This allows us to multiply by two the emulated drain capacitance per micrometer of W. Therefore half of W transistors can be used. This principle is shown in Fig. 15.

D. Integration Strategy

The integration of the peak-efficiency tracking algorithm relies on the accurate estimation of all resistive parasitic elements as the $R_L, R_H, R_{\rm PCB}, R_{\rm COIL}$, etc. The accuracy of these parameters is directly associated with the obtained accuracy of the peak-efficiency point detection.

The design of the peak-efficiency detection circuit follows the implementation of the schematic shown in Fig. 11 and includes all aspects discussed in previous sections (see Figs. 14, 15). During the circuit's validation, the parameters entering into (26) should be accurately verified; namely, the accuracy of $\alpha I_{\rm OUT}$, voltage $V_{N\_{\rm ON}\_{\rm AVG}}$, and resistance $R'_X = R_X$. All ohmic and dynamic powers can be extracted by the time-integral function of the graphical waveform viewer as shown in Fig. 4. This facilitates the verification of the peak-efficiency detection circuit.

Due to the tens of mV of $V_{N,P\_{\rm SWITCHON}\_{\rm AVG}}$ voltages, the voltage offset of all operational amplifiers is to be designed in a reasonable low range. However, as the low-speed operational amplifiers are required, obtaining low input offset voltage and low quiescent current can be easily achieved. Nevertheless, as we can see from the simulation shown in Fig. 17, the efficiency curves are relatively flat. On this account medium-accuracy design of the peak-efficiency detector is acceptable.

As the result of the integration, the top view of the integrated 5-A power stage is shown in Fig. 16. This power stage contains 20 PMOS and 20 NMOS segments. The control of the power-stage operation is provided by the analog chain containing amongst others the accurate zero-cross detector [14] and current sensor [12]. The power stage is equipped by Cu-pillar pads, ensuring low access resistance and low parasitic inductance of the power nets.

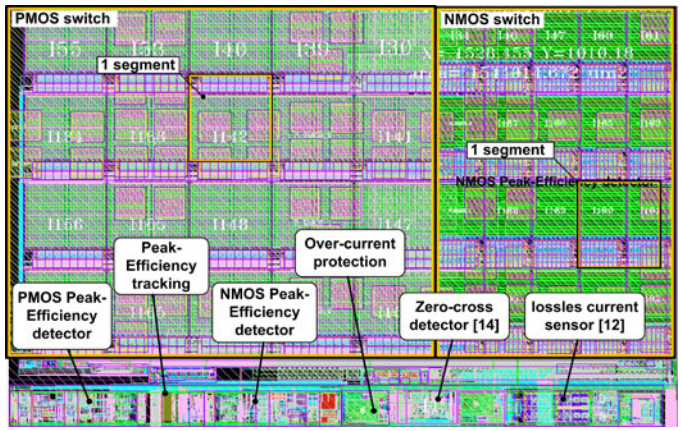

Fig. 16. Top view of the integrated 5 A power stage on 1000 μm $\times$ 1500 μm surface.

TABLE II
PARAMETERS OF THE STEP-DOWN DC–DC CONVERTER

DC-DC CONVERTER	VALUE
$V_{\rm DD}$ (V)	2.5 to 4.8
$V_{\rm OUT}$ (V)	0.6 to 1.8
$I_{\rm OUT\_MAX}$ (A)	5
$f_{\rm SW}$ (MHz)	3.2
L (µH)	1/0.47
PEAK-EFFICIENCY DETECTOR	
Quiescent current (µA) [1]	80
Area (µm^2)	87 × 750

[1] for $I_{\rm OUT}$ = 0A.

V. ALGORITHM RESULTS

The results presented here are obtained by the postlayout simulation on the previously described 5-A dc–dc converter power stage shown in Fig. 16. The partitioning and values of the parasitic elements used for simulation are listed in the footnote to Table I. The current consumption of the whole PMOS and NMOS peak-efficiency tracking system is below 100 μA ($I_{\rm OUT} = 0$). One iterative cycle (i.e., time where the peak-efficiency detection and following decision is performed) was set to three main clock cycles $T_{\rm CLK}$ ($\sim 0.94\ \mu$s). This ensures good stability of the control loop in Fig. 13. The main parameters of the dc–dc converters are resumed in Table II.

The main outcome of the peak-efficiency tracking algorithm is shown on the example of low duty-cycle operation in Fig. 17. The characteristics were obtained by a linear sweep of the output current $I_{\rm OUT}$ from 0 A $\rightarrow$ 5 A in $t = 1$ ms. Together with the peak-efficiency envelope, this figure also contains the power-efficiency obtained with fixed- minimal size ($4 \times N$, $4 \times P$) and maximal 100% size ($20 \times N$, $20 \times P$) power stages. This allows us to evaluate the gain of the optimization, which is in order of unit of% in a wide output current range. From the characteristics shown in Fig. 17, we also notice that the tuning of the NMOS and PMOS transistors' sizes is not simultaneous for this particular case, 4.8 $-$ 0.6 V.

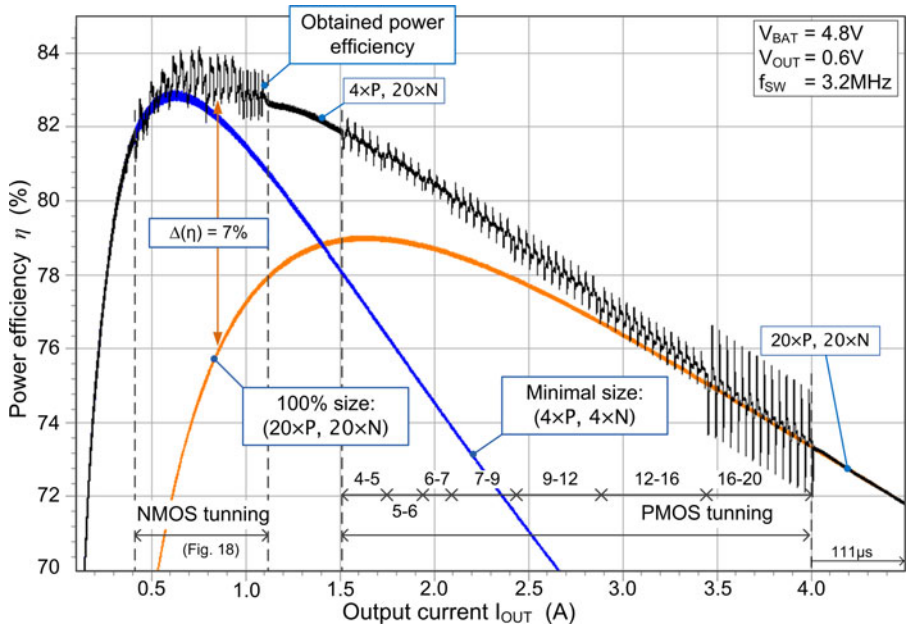

Fig. 17. Result of the peak-efficiency tracking on 5 A dc–dc buck converter. For comparison, efficiencies of the fixed-size power stages are also added.

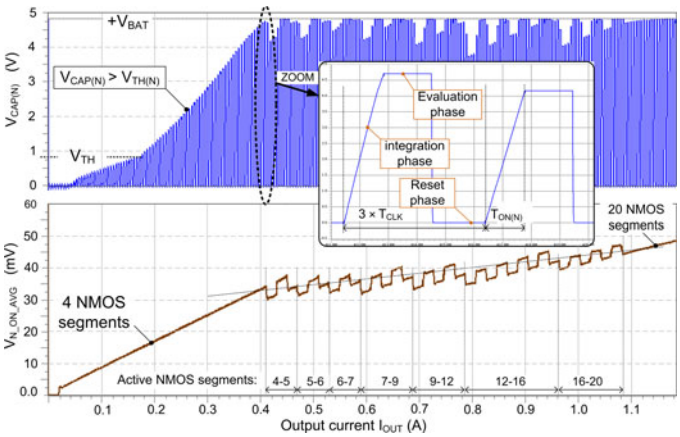

Fig. 18. Internal nodes $V_{\mathrm{CAP}(N)}$ and $V_{N\_\mathrm{ON}\_\mathrm{AVG}}$ for the NMOS peak-efficiency detection circuit simulation from Fig. 17.

In order to demonstrate the behavior inside the peak-efficiency detection circuit in Fig. 11, following Fig. 18 details the voltages $V_{N\_\mathrm{ON}\_\mathrm{AVG}}$ and $V_{\mathrm{CAP}(N)}$ for the identical condition as Fig. 17 simulation. In this figure, we notice that V_{DS} voltage of the power NMOS transistor is maintained in almost constant values, as explained in Section II-B. However, due to the effect of nonconstant drain capacitance (described in Section II-C) the $V_{N\_\mathrm{ON}\_\mathrm{AVG}}$ value slightly increases with output current I_{OUT}.

VI. Conclusion

In this paper, analysis of the dominant lossy contributors of the switched-mode power stage has been provided. Consequently, the methodology allowing us to detect the peak-efficiency operations of the periodically switching power MOS transistor has been defined. The circuit implementing the peak-efficiency tracking algorithm was used to optimize the mid-current efficiency of the 5 A step-down dc–dc converter operation with $f_{\mathrm{SW}} = 3.2$ MHz. The main field of the applications of the presented peak-efficiency tracking system is the optimization of the high-output current dc–dc converters, where the power gain can reach tens of milliwatt. Especially, power converters operating in wide input– output voltage range (i.e., with wide duty-cycle range) are concerned. As a result of the peak-efficiency tracking algorithm, increased life time of battery-operated devices can be obtained.

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